REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, claims 1, 5, 6, 8, 17, 19, 20, 27, and 36 have been amended, claims 4 and 23 canceled without prejudice or disclaimer for filing in a continuation application, and new figures 26-32 have been added. Thus, claims 1, 3, 5-6, 8-20, 22, 24-25, and 27-39 are currently pending in the application and subject to examination.

In the Office Action mailed December 19, 2002, the drawings were objected to; claims 1, 8, 17, 19, 27 and 36 were objected to because of certain informalities; claims 4-6, 14, 15, 23-25, 33, 34, 38 and 39 were rejected under 35 U.S.C. § 112, first paragraph; and claims 1, 3-6, 8-20, 22-25, and 27-39 were rejected under 35 U.S.C. § 112, second paragraph. Furthermore, claims 1, 3, 8-14, and 16 were rejected under 35 U.S.C. § 103(a), as being unpatentable over admitted prior art (Figs. 2-4) in view of U.S. Patent No. 5,903,513 to Itou. Claims 17, 18, 22, 27-33, and 35 were rejected under 35 U.S.C. § 103(a), as being unpatentable over admitted prior art (Figs. 2-4) in view of Itou, and further in view of U.S. Patent No. 6,232,810 to Oklobdzija et al. Applicants acknowledge with gratitude the indication that subject matter of claims 19, 20, 36, and 37 is allowable.

Objection to the Drawings

The drawings stand objected to as not showing every feature of the invention specified in the claims. Responsive to this rejection, new drawings 26-32 have been submitted. No new matter has been entered.

The new Figs. 26-32 are similar to drawings 8-9 and 13-17, but include the transistor 30' of Fig. 11A, which is supplied with the current control signal CCS. Applicants note that the specification states, at page 20, lines 6-10, that "the fourth to eighth embodiments described above, like the third embodiment shown in Fig. 11A, can also be so configured that a single transistor 30' having the gate thereof supplied with the current control signal CCS functions as both the transistor 30 and the transistor 3." New Figs. 26-32 illustrate exactly such configurations. Thus no new matter has been entered by adding new drawings 26-32.

New Fig. 26 shows a differential amplifier which includes a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit, and also including a fourth transistor, as recited in claims 1 and 5-6. Support for this drawing can be found, for example, in claims 1 and 5-6; in Figs. 8, 11A and 11B; and in the specification, at page 12, line 15 through page 13, line 20, at page 16, lines 1-34, and at page 20, lines 6-10.

New Fig. 27 shows a differential amplifier which includes a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit, and also including a fifth transistor, as recited in claims

11 and 30. Support for this drawing can be found, for example, in claims 11 and 30; in Figs. 9, 11A and 11B; and in the specification, at page 13, lines 21-35, at page 16, lines 1-34, and at page 20, lines 6-10.

New Fig. 28 shows a differential amplifier which includes a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit, and also including a sixth transistor, as recited in claims 12-13 and 31-32. Support for this drawing can be found, for example, in claims 12-13 and 31-32; in Figs. 13, 11A and 11B; and in the specification, at page 17, line 29 through page 18, line 27, at page 16, lines 1-34, and at page 20, lines 6-10.

New Fig. 29 shows a differential amplifier which includes a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit, and also including a seventh transistor, as recited in claims 14 and 33. Support for this drawing can be found, for example, in claims 14 and 33; in Figs. 14, 11A and 11B; and in the specification, at page 18, line 28 through page 19, line 8, at page 16, lines 1-34, and at page 20, lines 6-10.

New Fig. 30 shows a differential amplifier which includes a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit, and also including a fifth transistor, as recited in claims 11 and 30, and a seventh transistor, as recited in claims 14 and 33. Support for this drawing can be found, for example, in claims 11, 14, 30, and 33; in Figs. 15, 11A and

11B; and in the specification, at page 19, lines 9-18, at page 16, lines 1-34, and at page 20, lines 6-10.

New Fig. 31 shows a differential amplifier which includes a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit, and also including a sixth transistor, as recited in claims 12-13 and 31-32, and a seventh transistor, as recited in claims 14 and 33. Support for this drawing can be found, for example, in claims 12-14 and 31-33; in Figs. 16, 11A and 11B; and in the specification, at page 19, lines 9-24, at page 16, lines 1-34, and at page 20, lines 6-10.

New Fig. 32 shows a differential amplifier which includes a third transistor for keeping a minute current to flow through said first and second transistors, and wherein the third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit, and also including an eighth transistor, as recited in claims 15, 34, 38, and 39. Support for this drawing can be found, for example, in claims 15, 34, 38, and 39; in Figs. 17, 11A and 11B; and in the specification, at page 19, line 25 through page 20, line 5, at page 16, lines 1-34, and at page 20, lines 6-10.

As discussed above, Figs. 26-32 show every feature of the invention recited in the claims. Therefore, Applicants respectfully request reconsideration and withdrawal of the objection to the drawings.

Objections to the Claims

Claims 1, 8, 17, 19, 27, and 36 stand objected to because of certain formalities. These claims have been amended responsive to the objection. Accordingly, Applicants respectfully request withdrawal of the objection.

Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Applicants note that it is disclosed at page 20, lines 6-10, that "the fourth to eighth embodiments described above, like the third embodiment shown in Fig. 11A, can also be so configured that a single transistor 30' having the gate thereof supplied with the current control signal CCS functions as both the transistor 30 and the transistor 3." Claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39 recite exactly such configurations. In addition, the specification has been amended to include drawings of the differential amplifier circuits of claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39, and associated detailed descriptions. Therefore, claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39 comply with the written description requirement. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, first paragraph.

Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 1, 3-6, 8-20, 22-25, and 27-39 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 1-6, 8-20, 22-25, and 27-39 stand rejected as indefinite for including the term "minute current." In making this assertion, the Examiner states that "'minute'... is a relative term and the specification does not specifically indicate at which current value is considered to be 'minute current.' Therefore, it is now know how large/small of a current value to meet the limitation 'minute current' in the claim." This assertion is respectfully traversed.

Applicants concur that "minute" is indeed a relative term. However, Applicants note that the minute current is small relative to the drive current. Applicants further note that the current control signal CCS used to control the current of transistor 30' is depicted in Fig. 12. The accompanying description states that "by supplying a signal of high level 'H' to the gate of the transistor 30' at the same timing as the clock CK, a drive current is supplied to the circuit...Also, at the timing when the clock CK is reduced to the low level 'L', the gate of the transistor 30' is supplied with the current control signal CCS of intermediate level 'M', and a minute current is supplied to the circuit." Therefore, applying the known current control signal CCS of Fig. 12 to the transistor 30' results in a minute current and a drive current. One of ordinary skill in the art would be able to apply the known current control signal CCS of Fig. 12 to the transistor 30' to obtain the minute current and the drive current. Therefore, one of ordinary skill in the art would understand the definition of the "minute current" relative to the drive current. Accordingly, Applicants request withdrawal of the rejection under 35 U.S.C. § 112, second paragraph.

Claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39 stands rejected as indefinite for being misdescriptive. In making this assertion, the Examiner states "that there is no

such circuit corresponding to" each of these claims. Applicants note that it is disclosed at page 20, lines 6-10, that "the fourth to eighth embodiments described above, like the third embodiment shown in Fig. 11A, can also be so configured that a single transistor 30' having the gate thereof supplied with the current control signal CCS functions as both the transistor 30 and the transistor 3." Claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39 recite exactly such configurations. In addition, the specification has been amended to include drawings of the differential amplifier circuits of claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39, and associated detailed descriptions. Therefore, claims 4-6, 14, 15, 23-25, 33, 34, 38, and 39 are not misdescriptive. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of these claims under 35 U.S.C. § 112, first paragraph.

Rejections Under 35 U.S.C. § 103(a)

Claims 1, 3, 8-14, and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art (Figs. 2-4) in view of Itou. Claim 1 as amended recites in part:

> a fourth transistor for supplying a drive current at the time of signal determination in said differential amplifier circuit is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected; and
> said third transistor is connected in parallel to said fourth transistor.

Applicants have carefully reviewed the cited art and could find no disclosure or suggestion of a fourth transistor for supplying a drive current at the time of signal determination in the differential amplifier circuit inserted between the first power line and the common node to which the first electrodes of the first and second transistors are

connected. Furthermore, Applicants could find no disclosure or suggestion of the third transistor connected in parallel to the fourth transistor. Accordingly, none of the cited art, singularly or in combination, teaches or suggests the claimed invention, specifically the combination of a fourth transistor for supplying a drive current at the time of signal determination in the differential amplifier circuit inserted between the first power line and the common node to which the first electrodes of the first and second transistors are connected, and the third transistor connected in parallel to the fourth transistor. For at least this reason, Applicants submit that claim 1, as amended, is allowable over the cited prior art. As claim 1 is allowable over the cited prior art, Applicants submit that claims 3, 8-14, and 16, which depend from allowable claim 1, are likewise allowable over the cited prior art.

Claims 17, 18, 22, 27-33, and 35 stand rejected under 35 U.S.C. § 103(a), as being unpatentable over Applicants' admitted prior art (Figs. 2-4) in view of Itou, and further in view of Oklobdzija. Claim 17 has been amended to include the features of claim 23. For similar reasons to those discussed with regard to claim 1, Applicants submit that claim 17, as amended, is allowable over the cited prior art. As claim 17 is allowable over the cited prior art, Applicants submit that claims 18, 22, 27-33, and 35, which depend from allowable claim 17, are likewise allowable.

Conclusion

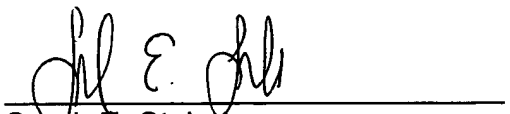
Applicants' amendments and remarks have overcome the objections and rejections set forth in the Office Action dated December 1, 2003. Specifically, Applicants' remarks have pointed out each feature of the invention specified in the

claims in one of the figures and thus overcome the objection of the drawings under 37 C.F.R. § 1.83(a). Applicants' amendments to claims 1, 8, 17, 19, 27, and 36 have overcome the objections to these claims. New Figs, amendments to the specification, and Applicants' remarks have overcome the rejections under 35 U.S.C. § 112, first paragraph and 35 U.S.C. § 112, second paragraph. Applicants' remarks regarding claims 1 and 17 have overcome the rejections under 35 U.S.C. § 103(a).

Applicants respectfully submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that any additional fees are due with respect to the filing of this paper, the undersigned authorizes the Office to charge any additional fees to our Deposit Account No. 01-2300, making reference to Docket No. 100021-00069.

Respectfully submitted,



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Enclosures: Petition for Extension of Time, Figs. 26-32.